

What Is Claimed Is:

1 1. A logic system with adaptive supply voltage control,
2 comprising:
3 a logic circuit clocked by a clock signal of a
4 predetermined frequency generated by a clock generating
5 circuit, said logic circuit having a critical path delay
6 being equal to or shorter than a period of the clock signal;
7 and
8 a voltage conversion circuit for dynamically regulating
9 a supply voltage for powering said logic circuit based on
10 a bias voltage of the clock generating circuit.

1 2. The logic system with adaptive supply voltage
2 control of claim 1, wherein the clock generating circuit
3 comprises an oscillator and wherein the period of the clock
4 signal is equal to two times of a loop delay of the
5 oscillator.

1 3. The logic system with adaptive supply voltage
2 control of claim 1, wherein the clock generating circuit
3 comprises an oscillator and a divide-by-k divider connected
4 at the output of the oscillator, and wherein the period of
5 the clock signal is equal to 2 times of a loop delay of the
6 oscillator times k.

1 4. The logic system with adaptive supply voltage
2 control of claim 1, wherein the period of the clock signal
3 is longer than said critical path delay of said logic
4 circuit.

1 5. The logic system with adaptive supply voltage
2 control of claim 1, wherein the supply voltage for powering
3 said logic circuit is dynamically regulated such that said

4 critical path delay of said logic circuit approximately
5 matches the period of the clock signal.

1 6. The logic system with adaptive supply voltage
2 control of claim 1, wherein said voltage conversion circuit
3 comprises a voltage regulator.

1 7. The logic system with adaptive supply voltage control
2 of claim 1, wherein said voltage conversion circuit
3 comprises a DC-DC converter.

1 8. The logic system with adaptive supply voltage
2 control of claim 1, wherein a delay matching circuit is
3 employed to achieve matching between said critical path
4 delay of said logic circuit and the period of the clock
5 signal.

1 9. The logic system with adaptive supply voltage control
2 of claim 1, wherein a DLL (delay-locked loop) circuit is
3 employed to achieve matching between said critical path
4 delay of said logic circuit and the period of the clock
5 signal.

1 10. A logic system with adaptive supply voltage control,
2 comprising:

3 a logic circuit having a power supply terminal for
4 receiving a supply voltage and a clock input terminal for
5 receiving a clock signal of a predetermined frequency from
6 a clock generating circuit, said logic circuit having
7 similar delay characteristics with the clock generating
8 circuit; and

9 a voltage conversion circuit for dynamically regulating
10 the supply voltage at said power supply terminal of said
11 logic circuit on the basis of a bias voltage of the clock

12 generating circuit.

1 11. The logic system with adaptive supply voltage
2 control of claim 10, wherein the clock generating circuit
3 comprises an oscillator and wherein a period of the clock
4 signal is equal to two times of a loop delay of the
5 oscillator.

1 12. The logic system with adaptive supply voltage
2 control of claim 10, wherein the clock generating circuit
3 comprises an oscillator and a divide-by-k divider connected
4 at the output of the oscillator, and wherein a period of the
5 clock generating circuit is equal to two times of a loop delay
6 of the oscillator times k.

1 13. The logic system with adaptive supply voltage
2 control of claim 10, wherein a period of the clock signal
3 is slightly longer than a critical path delay of said logic
4 circuit.

1 14. The logic system with adaptive supply voltage
2 control of claim 10, wherein the regulated supply voltage
3 at said power supply terminal of said logic circuit is higher
4 than the bias voltage of the clock generating circuit.

1 15. The logic system with adaptive supply voltage
2 control of claim 10, wherein the regulated supply voltage
3 at said power supply terminal of said logic circuit is equal
4 to the bias voltage of the clock generating circuit.

1 16. The logic system with adaptive supply voltage
2 control of claim 10, wherein said voltage conversion circuit
3 comprises a voltage regulator.

1 17. The logic system with adaptive supply voltage
2 control of claim 10, wherein said voltage conversion circuit
3 comprises a DC-DC converter.

1 18. The logic system with adaptive supply voltage
2 control of claim 10, wherein logic elements constituting
3 said logic circuit have similar delay sensitivity to supply
4 voltage, temperature and process shifts with delay elements
5 in the clock generating circuit.

1 19. An adaptive supply voltage control method for a logic
2 circuit clocked by a clock signal of a predetermined
3 frequency from a clock generating circuit, said logic
4 circuit having a critical path delay being equal to or shorter
5 than a period of the clock signal, said method comprising
6 dynamically regulating a supply voltage for powering said
7 logic circuit based on a bias voltage of the clock generating
8 circuit.

1 20. The adaptive supply voltage control method of claim
2 19, wherein the supply voltage for powering said logic
3 circuit is dynamically regulated such that said critical
4 path delay of said logic circuit approximately matches the
5 period of the clock signal.

1 21. An adaptive supply voltage control method for a logic
2 circuit clocked by a clock signal of a predetermined
3 frequency from a clock generating circuit, said logic
4 circuit having similar delay characteristics with the clock
5 generating circuit, said method comprising dynamically
6 regulating a supply voltage for said logic circuit on the
7 basis of a bias voltage of the clock generating circuit.

1 22. The adaptive supply voltage control method of claim
2 21, wherein a period of the clock signal is longer than a
3 critical path delay of said logic circuit.

1 23. The adaptive supply voltage control method of claim
2 21, wherein the regulated supply voltage for said logic
3 circuit is equal to or higher than the bias voltage of the
4 clock generating circuit.